

WHAT IS CLAIMED IS:

1. A pre-pit signal decoder, comprising:
 - a shift register for receiving serial pre-pit bits and converting them into a parallel pre-pit byte;
 - 5 a pattern comparator for generating an odd sync bit, an even sync bit, a low bit, and a high bit according to the parallel pre-pit byte, the pattern comparator further receiving a disable signal and operating when the disable signal is not enabled;
 - a counting unit for generating a counting value according to the odd sync bit, the even sync bit, the low bit, and the high bit, and marking evenness or oddness of frames of the pre-pit bit and sequence of wobble signals in the frames;
 - 10 an in-sync signal generating unit for generating an in-sync signal according to the odd sync bit, the even sync bit, the low bit, and the high bit; and
 - 15 a protection unit for receiving the counting value and the in-sync signal, and enabling the disable signal at positions where the pre-pit bits do not exist according to the counting value of the counting unit when the in-sync signal is enabled.
2. The pre-pit signal decoder according to claim 1, wherein the counting unit comprises:
 - 20 an OR gate for receiving the odd sync bit, the even sync bit, the low bit and the high bit, and generating a find-bit signal;

a first counter for counting a wobble signal reference clock and outputting a wobble signal counting value, and utilizing the find-bit signal to clear the counting value; and

5 a second counter for receiving outputs of the first counter, the odd sync bit and the even sync bit, adding one after the first counter has counted a number of the wobble signals contained in the frames, and outputting a frame counting value, wherein the second counter sets a lowest bit of the frame counting value to H when the odd sync bit is found, and to L when the even sync bit is found.

- 10 3. The pre-pit signal decoder according to claim 2, wherein the protection unit enables the disable signal when the in-sync signal is enabled and the wobble signal counting value is smaller than 5.
4. The pre-pit signal decoder according to claim 2, wherein the in-sync signal generating unit is a finite state machine.
- 15 5. The pre-pit signal decoder according to claim 4, wherein the finite state machine further generates a find even position signal.
6. The pre-pit signal decoder according to claim 5, wherein the protection unit enables the disable signal when the in-sync signal is enabled and the find even position signal is enabled, and disables the disable signal when 1 is
- 20 added to the frame counting value.
7. The pre-pit signal decoder according to claim 1, wherein the pre-pit byte is 8-bit data.

8. The pre-pit signal decoder according to claim 7, wherein the pattern comparator compares the pre-pit byte to a plurality of 8-bit reference patterns when the in-sync signal is not enabled.
9. The pre-pit signal decoder according to claim 8, wherein:
 - 5 the reference patterns are 00000111, 00000110, 00000101 and 00000100; when the pre-pit byte is the same as the reference pattern 00000111, the even sync bit is set to high level; when the pre-pit byte is the same as the reference pattern 00000110, the odd sync bit is set to high level; when the pre-pit byte is the same as the reference pattern 00000101, the high bit is set to high level; and when the pre-pit byte is the same as the reference pattern 00000100, the low bit is set to high level.
 10. The pre-pit signal decoder according to claim 7, wherein the pattern comparator compares lower 3-bit data of the pre-pit byte to a plurality of 3-bit reference patterns when the in-sync signal is enabled.
 11. The pre-pit signal decoder according to claim 10, wherein:
 - 15 the reference patterns are 111, 110, 101 and 100; when the lower 3-bit data of the pre-pit byte is the same as the reference pattern 111, the even sync bit is set to high level; when the lower 3-bit data of the pre-pit byte is the same as the reference pattern 110, the odd sync bit is set to high level;

when the lower 3-bit data of the pre-pit byte is the same as the reference pattern 101, the high bit is set to high level; and

when the lower 3-bit data of the pre-pit byte is the same as the reference pattern 100, the low bit is set to high level.

5 12. The pre-pit signal decoder according to claim 1, wherein the pattern comparator further generates a data ready signal.

10 13. The pre-pit signal decoder according to claim 12, further comprising an output unit for receiving the odd sync bit, the even sync bit, the low bit, the high bit, and the data ready signal, and converting the serial low bit and high bit into pre-pit data for output according to the data ready signal, the odd sync bit and the even sync bit.

14. The pre-pit signal decoder according to claim 7, wherein the pattern comparator compares lower 2-bit data of the pre-pit byte to a plurality of 2-bit reference patterns when the in-sync signal is enabled.

15 15. The pre-pit signal decoder according to claim 14, wherein:

the reference patterns are 11, 10, 01 and 00;

when the lower 2-bit data of the pre-pit byte is the same as the reference pattern 11, the even sync bit is set to high level;

20 when the lower 2-bit data of the pre-pit byte is the same as the reference pattern 10, the odd sync bit is set to high level;

when the lower 2-bit data of the pre-pit byte is the same as the reference pattern 01, the high bit is set to high level; and

when the lower 2-bit data of the pre-pit byte is the same as the reference pattern 00, the low bit is set to high level.

16. A pre-pit decoding circuit for receiving a pre-pit signal and a wobble signal and outputting a pulse signal and a new pre-pit signal, comprising:

a pulse generating unit for generating the pulse signal, wherein the pulse signal rises substantially at the same time as the wobble signal rises;

an extension unit for generating an extension signal which rises substantially at the same time as the pre-pit signal rises and falls substantially at the same time as the pulse signal falls; and

an AND-operation unit for generating the new pre-pit signal by doing an AND-operation on the extension signal and the pulse signal.

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Rest of Claim 15 and Claim 16.